are arranged two-dimensionally in a plurality of rows and in a plurality of columns and in one-to-one correspondence with the plurality of photodetectors in the photodetector array, each processing element performing a predetermined calculation on digital signals which are transferred from the analog-to-digital converter array; a column-direction data-transfer bus including a plurality of column-direction data-transfer data lines which are arranged in one to one correspondence with the plurality of columns in the parallel processing system, each column-direction data-transfer data line being connected to the processing elements that are located in the corresponding column and performing data transfer operation with each processing element in the corresponding column; a row-direction data-transfer bus including a plurality of row-direction data-transfer data lines which are arranged in one to one correspondence with the plurality of rows in the parallel processing system, each row-direction data-transfer data line being connected to the processing elements that are located in the corresponding row and performing data transfer operation with each processing element in the corresponding row; and a control circuit controlling the photodetector array, the analog-to-digital converter array, the parallel processing system, the column-direction data-transfer bus, and the row-direction data-transfer bus, and performing data transfer operation with the processing elements via the column-direction data-transfer bus and the row-direction data-transfer bus, the control circuit controlling a combination of data to be transferred via each column-direction data-transfer data line to the corresponding processing elements and data to be transferred via each row-direction data-transfer data line to the corresponding processing elements, thereby controlling each processing element to perform a processing that is determined based on the combination of data received from the corresponding column-direction data-transfer data line and data received from the corresponding row-direction data-transfer data line.

Page 6, lines 9-25 and Page 7, lines 1-3, delete current paragraph and insert therefor:

For example, it is preferable that the control circuit includes a center-of-gravity calculation control portion for controlling each column-direction data-transfer data line to perform data transfer operation to transfer data indicative of positional information of the corresponding column to the processing elements on the corresponding column, for controlling each row-direction data-transfer data line to perform data transfer operation to transfer data indicative of positional information of the corresponding row to the processing elements on the corresponding row, and for controlling each processing element to perform a predetermined calculation to calculate a center of gravity of the digital signals based on the received data indicative of the positional information of the corresponding row and the received data indicative of the postional information of the corresponding column. Because the dedicated data buses are provided both in the column direction and in the row direction, it is possible to efficiently transfer the positional information by using a small number of data-transfer line systems. The positional information is required for performing the center-of-gravity calculation, which is a basic calculation for image processings.

Page 7, lines 6-14, delete current paragraph and insert therefor:

For example, it is preferable that the control circuit includes a control portion for controlling a predetermined processing element to perform a predetermined calculation onto the digital signals by controlling a column-direction data-transfer data line that is connected to the predetermined processing element and a row-direction data-transfer data line that is connected to the predetermined processing element to perform data transfer operation to transfer a predetermined combination of calculation-control data. In this case, it is possible to control individual processing elements to perform different calculation operations.

Page 7, lines 15-25, delete current paragraph and insert therefor:

It is preferable that the control circuit includes a data transfer control portion. In this case, it becomes possible to transfer a calculation result obtained at some particular-

processing element to the control circuit for controlling a column-direction data-transfer data line that is connected to a predetermined processing element and a row-direction data-transfer data line that is connected to the predetermined processing element to perform data transfer operation to transfer a predetermined combination of calculation-control data, thereby allowing calculation result data, obtained at the predetermined processing element, to be transferred to the control circuit.

Page 8, lines 13-25 and Page 9, lines 1-7, delete current paragraph and insert therefor:

It is preferable that the parallel processing system further includes a shift register array, the shift register array having a plurality of shift registers which are disposed in one-to-one correspondence with the plurality of analog-to-digital converters and in one-to-one correspondence with the plurality of rows of processing elements, each shift register successively transferring digital signals, which are outputted from the corresponding analog-to-digital converter and which are equivalent to signals outputted from the photodetectors in a corresponding photodetector row, to predetermined processing elements in the corresponding row. The shift registers are used as being dedicated to transferring data to the processing elements. Accordingly, calculation processing can be performed even during the transfer process. Processing can be performed efficiently by reducing the wait time for both of the transfer process and the calculation process, thereby reducing the overall processing time. It is possible to achieve a pipeline operation, and to perform a high-speed image processing, and particularly real-time processing. According to another aspect, the present invention provides a high-speed vision sensor, comprising: a photodetector array having a plurality of photodetectors, which are arranged two-dimensionally in a plurality of rows and in a plurality of columns; an analog-to-digital converter array having a plurality of analog-to-digital converters which are arranged one-dimensionally such that each analog-to-digital converter corresponds to one row in the photodetector array, each analog-to-digital converter

converting, into digital signals, analog signals which are successively outputted from the photodetectors in the corresponding row; a parallel processing system including a parallel processing element array, the parallel processing element array having a plurality of processing elements which are arranged two-dimensionally in a plurality of rows and in a plurality of columns and in one-to-one correspondence with the plurality of photodetectors in the photodetector array, each processing element performing a predetermined calculation on digital signals which are transferred from the analog-to-digital converter array; a column-direction data-transfer bus including a plurality of column-direction data-transfer data lines which are arranged in one to one correspondence with the plurality of columns in the parallel processing system, each column-direction data-transfer data line being connected to the processing elements that are located in the corresponding column and performing data transfer operation with each processing element in the corresponding column; a row-direction data-transfer bus including a plurality of row-direction data-transfer data lines which are arranged in one to one correspondence with the plurality of rows in the parallel processing system, each row-direction data-transfer data line being connected to the processing elements that are located in the corresponding row and performing data transfer operation with each processing element in the corresponding row; and a control circuit controlling the photodetector array, the analog-to-digital converter array, the parallel processing system, the column-direction data-transfer bus, and the row-direction data-transfer bus, and performing data transfer operation with the processing elements via the column-direction data-transfer bus and the row-direction data-transfer bus, the control circuit receiving data from each processing element via both of the corresponding column-direction data-transfer data line and the corresponding row-direction data-transfer data line, and determining the position of a processing element that has outputted predetermined data, based on the combination of a